

AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

5       depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tungsten containing film;

10       depositing a second metal layer overlying said etch stop layer;

          etching through said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

15       thereafter etching ~~partially~~ through said second metal layer to form vias;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

20 polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

2. (Currently Amended) The method according to Claim 1 wherein said first and second metal layer layers comprises one of the group of: aluminum, aluminum alloys, tungsten and copper.

3. (Original) The method according to Claim 1 wherein said semiconductor substrate comprises semiconductor devices in and on a silicon substrate covered by an insulating layer.

4. (Canceled)

5. (Original) The method according to Claim 1 wherein said dielectric layer comprises one of the group of:  $\text{SiO}_2$ ,  $\text{SiOF}$  (fluorinated silica glass),  $\text{SiOC}$  (C-substituted siloxane), amorphous  $\text{SiC:H}$ ,  $\text{MSQ}$  (methylsilsesquioxane), porous

5        materials, PPXC polymer (poly(chloro-p-xylylene), PPXN  
polymer (poly-p-xylylene), and VT-4 (tetrafluoro-p-  
xylylene).

6. (Original) The method according to Claim 1 wherein said dielectric layer is deposited to a thickness of between about 5,000 Angstroms and 20,000 Angstroms.

7. (Currently Amended) The method according to Claim 1 further comprising depositing an anti-reflective coating layer overlying said second metal layer prior to said step of etching through said second metal layer to form  
5        connective lines.

8. (Currently Amended) The method according to Claim 7 1  
~~wherein said further comprising depositing an anti-~~  
~~reflective coating layer overlying said second metal layer~~  
~~wherein said anti-reflective coating layer comprises~~  
5        ~~titanium nitride (TiN) and wherein said anti-reflective~~  
~~coating layer is a polishing stop for said step of~~  
~~polishing down said dielectric layer.~~

9. (Currently Amended) A method of forming self-aligned,

anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

5 depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tantalum containing film;

10 depositing a second metal layer overlying said ~~first metal layer etch stop layer~~;

~~depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer,~~

15 etching through ~~said anti-reflective coating layer,~~ said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

thereafter etching through ~~said anti-reflective coating layer and said second metal layer~~ to form vias;

20 thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective 25 coating layer is a polishing stop.

10. (Original) The method according to Claim 9 wherein said first metal layer and said second metal layer comprise one of the group of: aluminum, aluminum alloys, tungsten and copper.

11. (Original) The method according to Claim 9 wherein said first metal layer is deposited to a thickness of between about 1,000 Angstroms and 10,000 Angstroms.

12. (Original) The method according to Claim 9 wherein said second metal layer is deposited to a thickness of between about 3,000 Angstroms and 10,000 Angstroms.

13. (Canceled)

14. (Canceled)

15. (Currently Amended) The method according to Claim 14 9 wherein said step of etching through ~~said ARC layer and~~ said second metal layer to form vias has an endpoint at said etch stop layer.

16. (Canceled)

17. (Original) The method according to Claim 9 wherein said dielectric layer comprises one of the group of: SiO<sub>2</sub>, SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane),  
5 porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), and VT-4 (tetrafluoro-p-xylylene).

18. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;  
5 depositing a first metal layer overlying said semiconductor substrate;  
depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tantalum containing film;  
10 depositing a second metal layer overlying said first metal layer;  
depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;  
etching through said anti-reflective coating layer,

15 said second metal layer, said etch stop layer, and said second metal layer to form connective lines;

thereafter etching through said anti-reflective coating layer and said second metal layer to form vias wherein said etch stop layer acts as an etch stop;

20 thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of 25 the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

19. (Original) The method according to Claim 18 wherein said first metal layer and said second metal layer comprise one of the group of: aluminum, aluminum alloys, tungsten, and copper.

20. (Original) The method according to Claim 18 wherein said first metal layer is deposited to a thickness of between about 1,000 Angstroms and 10,000 Angstroms.

21. (Original) The method according to Claim 18 wherein said second metal layer is deposited to a thickness of between about 3,000 Angstroms and 10,000 Angstroms.

22. (Canceled)

23. (Original) The method according to Claim 18 wherein said dielectric layer comprises one of the group of: SiO<sub>2</sub>, SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane),  
5 porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), and VT-4 (tetrafluoro-p-xylylene).